

COMPARISON OF TRAP STATES BETWEEN CIGSS/CdS/ZnO AND Cd PE CIGSS/ZnO CELLS

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ABSTRACT: In the continuing attempt to find an alternative to CdS windows for CIS absorbers, recent results show that a Cd-doped CIGS surface can produce a cell comparable to the best CdS/CIGS cells. We extend this work to include CIGSS-based cells utilizing the same absorber preparation process as is currently used to manufacture commercial photovoltaic modules. We use current-voltage, quantum efficiency, capacitance-frequency-temperature, and capacitance-voltage-temperature measurements to extract parameters and qualitative information pertaining to current transport in CIGSS-based cells. These cells have p-n junctions formed by either chemical-bath deposition of CdS or Cd-doping of the CIGSS using a partial electrolyte of Cd. In addition, we use the AMPS modeling software to investigate mechanisms of Cd-doping.
Keywords: CIS - 1: Cd doping - 2: Trapping Defects - 3

1. INTRODUCTION

Polycrystalline CIGS thin film photovoltaic cells are known for their high conversion efficiency [1] and are hence considered a viable option for producing solar-electric power at low cost. The best photovoltaic junctions are produced when a thin CdS layer is deposited by chemical-bath deposition. This is followed by the deposition of a wide band gap, transparent conducting oxide layer, ZnO, giving rise to the structure ZnO/CdS/CIGS. The properties of the CIGS thin films [2], and those of the CdS layer [3] have been studied separately. There are many "models" that attempt to explain the nature of the junction, but our view is that the primary factor governing the quality of the photovoltaic junction is the interaction of CdS with CIGS during the CdS deposition. Previous work on this subject [4,5] has shown that the environment in which the CdS is grown is sufficiently reactive to produce dissolution of species (Cu and Se), and to introduce appreciable amounts of Cd into the CIGS lattice. Experiments in which CuInSe_2 and $\text{CuIn}_{1-x}\text{Ga}_x\text{Se}_2$ (CIGS) thin films were treated in Cd solutions (Cd PE treatment) yielded solar cells with efficiencies comparable to those with CdS layers [4,5,6]. We attributed this to the n-type doping by Cd. In this report, we extend this work to S-containing absorbers, i.e. CIGSS thin film devices. In addition, modeling yields some introductory hypotheses regarding the ZnO/Cd PE treated CIGSS structure. Finally, we use admittance spectroscopy and drive-level capacitance profiling [7] to probe the spatial extent of the electronic effects of the Cd PE treatment.

2. EXPERIMENTAL DETAILS

2.1 Sample Preparation

The absorbers were grown on soda lime glass coated first with SiO_2 and then with Mo. The SiO_2 serves as a barrier to Na diffusion. Copper, gallium and indium precursors to CIGSS formation are deposited by sputtering. These

precursors are heated in H_2Se and H_2S to form the CIGSS absorber [8]. The resulting film is typically 1.2 μm thick. The film composition is $\text{CuIn}_x\text{Ga}_{1-x}(\text{Se}_y\text{S}_{1-y})_2$, and the band gap (extrapolated from QE measurements) of the absorbing region is approximately 1.07 eV. CdS layers were grown from an aqueous solution containing 0.0015M CdSO_4 , 1.5M NH_4OH , and 0.0075M thiourea at a maximum temperature of 65 °C for 15 min. ZnO films were deposited in two stages: the first layer from an undoped ZnO target, and the second and more conductive layer from an Al_2O_3 doped target to produce a total film thickness of 0.3 μm . For the Cd solution treatments, the procedure was similar to the CdS deposition, but the thiourea was omitted and the process temperature was slightly higher (75 °C, 30 min). This step is described as a "Cd partial electrolyte (Cd PE)" treatment. In addition, the Cd PE treatment was followed by an air anneal at 200 °C for 5 minutes to prevent shunting, a step which has not been necessary with the CdS devices.

2.2 Measurement Techniques

The current-voltage (JV), quantum efficiency and capacitance-voltage (CV) characteristics of six cells on each of two substrates were measured at room temperature and found to be consistent across each substrate. From these twelve cells, two samples were chosen to undergo admittance spectroscopy, the measurement of capacitance and conductance as a function of frequency and temperature. These samples were small sections of the cells on which room-temperature measurements were performed. Additionally, preliminary drive-level capacitance profiling (DLCP) measurements were made. These are essentially capacitance-voltage-temperature measurements in which both the ac and dc bias are modulated. The technique is relatively new to CIGS(S)-based cells and is described in more detail elsewhere [7,9].

3. RESULTS

3.1 Room-temperature Measurements

Fig. 1 compares typical JV characteristics of the two types of cells in the dark and under illumination. No significant variations were seen among devices of the same type. The Cd PE treated devices have respectable diode characteristics, as detailed in Table 1. Indeed, they are comparable to the CdS devices. This is encouraging, since these CIGSS-based cells were made utilizing the same absorber preparation process as is currently used to manufacture commercial photovoltaic modules. Thus we see the potential for commercial feasibility of a device with a CIGS(S) absorber without a CdS window layer.

CELL PARAMETERS

Table 1: Comparison of cell parameters extracted from illuminated JV measurements.

Cell	CdS Layer	Cd PE
η [%]	11.9	11.1
J_{sc} [mA/cm^2]	30.7	32.8
V_{oc} [mV]	564	521
FF [%]	68.8	65.0
A	[1.6]	2.2
R_s [$\text{U}\cdot\text{cm}^2$]	[1.3]	0.4
R_{shunt} [$\text{U}\cdot\text{cm}^2$]	1000	600

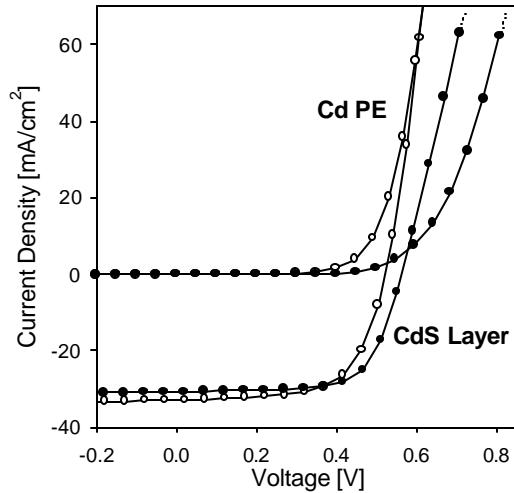


Fig. 1: JV of Cd PE device (open circles) and device with a CdS layer (filled circles). Measurements made at room temperature. Illumination was $100 \text{ mW}/\text{cm}^2$ for light JV measurements. Dotted lines are guides to the eye following the trend of the curves.

It is clear that the solar cells with the CdS buffer layer have somewhat superior voltage compared to the Cd PE treated devices. Note, however, that the Cd PE treated devices do not suffer from crossover of the illuminated and dark diode curves to the same extent as the CdS devices.

The internal quantum efficiency (IQE) comparison (Fig. 2) highlights the regions of superior current collection seen in Fig. 1. Not only does the current of the Cd PE devices benefit from the lack of a window layer with $E_g \sim 2.4 \text{ eV}$, it also benefits from greater collection in the longer wavelength region. Thus, although the Cd PE devices do have a weaker junction based on the JV curves, their

superior collection of red photons implies a longer collection length.

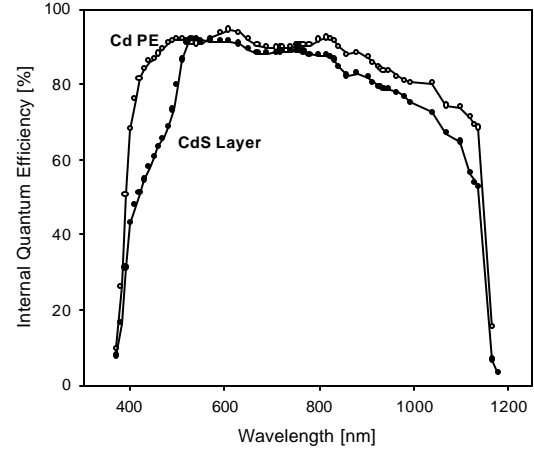


Fig. 2: Internal Quantum Efficiency of Cd PE device (open circles) and device with a CdS layer (filled circles). Measurements were taken without white light or voltage bias.

The CV results and extrapolated free hole densities (Fig. 3) show that while the absorber hole density far from the junction may not be significantly impacted by the window growth, the hole density in Cd PE cells increases near the junction. This suggests that the CdS cell is more compensated than the Cd PE cell near the junction.

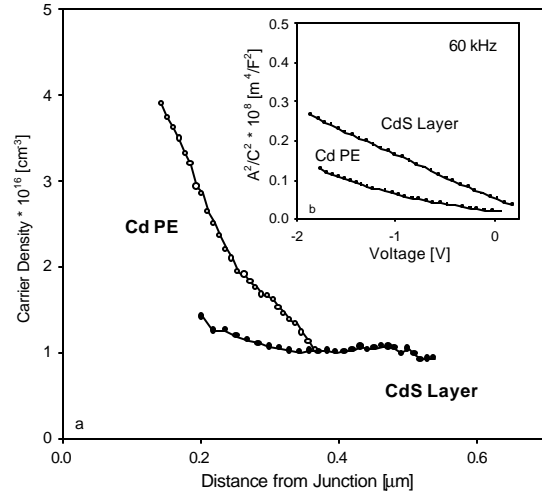


Fig. 3: Free hole density vs. distance from the electrical junction (a). Inset (b) is the room-temperature CV data from which the hole density was derived.

3.2 Modeling

Although the calculated JV curves in Fig. 4 are not a quantitative match to the experimental JV curves in Fig. 1, they do replicate the experimental trends. The models used to simulate the JV curves for both devices included an n-type CIGSS layer adjacent to the window layer(s). The more significant reduction in V_{oc} relative to the bandgap in the Cd PE device was accomplished by adding defects to this n-type CIGSS layer. The match to the crossover behavior (noticeable in the CdS device) was accomplished by the significant presence of deep acceptor-like defects in the n-type materials in the CdS device. The reduced

crossover seen in the modeled curves qualitatively similar to the Cd PE device was accomplished by simulating partial passivation of these same defects. Our experience in matching modeled curves to experimental curves with crossover using the AMPS modeling program [10] has consistently included these deep acceptor-like defects.

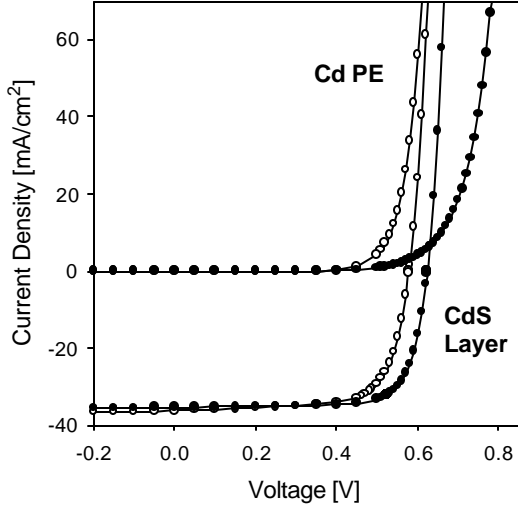


Fig. 4: Modeled JV curves intended to simulate experimental results from Cd PE devices (open circles) and devices with a CdS layer (filled circles).

These are important initial steps in helping to understand the mechanisms responsible for observed behavior. Future steps will involve looking more closely at the energies of the defects in the model as compared to defect energies predicted by first principles calculations for these specific materials.

3.3 Temperature-dependent Capacitance Measurements

Fig. 5 contains data from capacitance-frequency measurements taken at various temperatures for the two cells. Evidence of defects with similar time constants can be seen for both cells. The average trap-response frequency (deduced from the readily identifiable transitions from regions with to regions without trapping contributions to the capacitance) ranges from 0.5 - 80 kHz, thus the related time constants are near the μ s to ms range. However, the activation energies of the defects detected in this frequency-temperature space are different (Fig. 6).

The activation energies (E_a) were derived from the slopes shown in Fig. 6, as described in [11] and elsewhere. Hence, it again appears that the Cd PE and CdS processes have affected the absorber differently. It is interesting to note that other groups [11] have found that the defects with $E_a \sim 120$ meV can be transformed into defects with $E_a \sim 240$ meV using a 200 °C air anneal. Yet, in our experiments, the cell that had undergone the air anneal is the one that maintained the defects with the lower activation energy.

Drive-level capacitance profiling (DLCP) measurements complement the results of Fig. 6. Both the maximum and minimum defect densities detected by this technique are similar for the two cells. This suggests that although there are different diffusion mechanisms

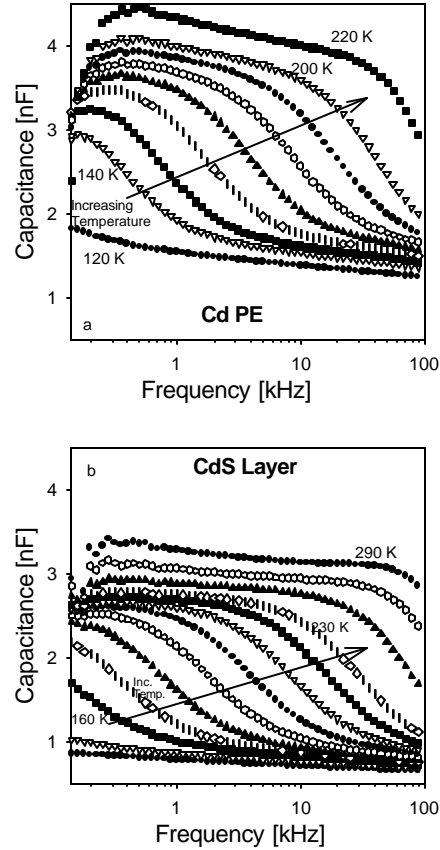


Fig. 5: Admittance Spectroscopy results for a Cd PE device (a) and a device with a CdS layer (b). Measurements were made in the 150K - 280K range at zero bias. Measurements in the center of the temperature range are at 10K intervals. Others are 20K intervals.

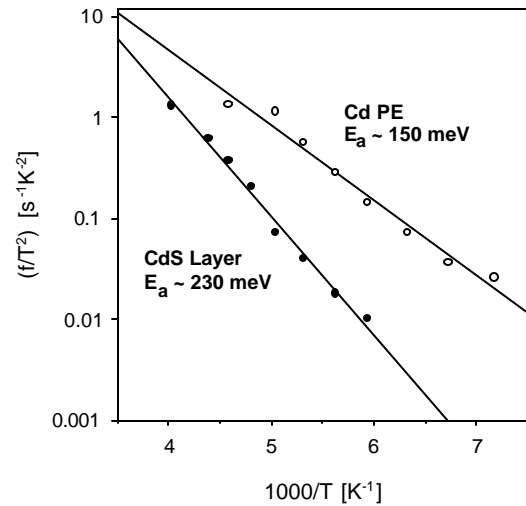


Fig. 6: Temperature-scaled average trap-response frequency (t/T^2) vs. inverse temperature.

depending on the process by which the junction is formed, they may move approximately the same number of ions able to passivate defects.

Fig. 7 plots the activation energies of the defects taken from Fig. 6. The spatial profile ranges were deduced from DLCP. Defects were found in relatively similar spatial locations with comparable densities for the two cells, and the defect densities were approximately constant over the spatial range profiled.

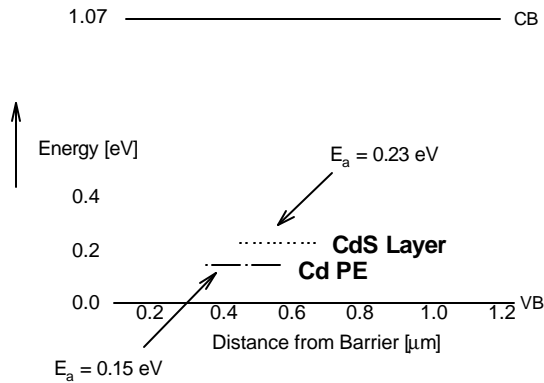


Fig. 7: Bandgap diagram representation of defects detected in admittance spectroscopy and DLCP measurements. Activation energies were determined from admittance spectroscopy. Spatial ranges are congruent with DLCP measurements.

4. DISCUSSION

A novel technique (Cd PE treatment) for the formation of p-n junctions in CIGS(S)-based solar cells may be commercially feasible in the near future. It has been successfully applied to cells that utilized the same absorber preparation process as is currently used to manufacture commercial photovoltaic modules. These cells maintained their diode characteristics after several months in storage at room temperature.

The Cd PE process resulted in cells with a weaker junction (lower V_{OC}), yet a longer collection length. This trade-off is suggestive of two mechanisms occurring during the Cd PE process -- one which fails to form as strong a junction as the CdS layer does, and another which improves voltage, as evidenced in the apparent longer collection length of the carriers, thereby offsetting some of the junction loss.

Admittance spectroscopy and DLCP coupled with room-temperature CV suggest that although Cd ions from the Cd PE process are having an effect on the electronic properties at least 0.5 μm into the CIGSS absorber, they are not diffusing into the same positions in the lattice. The CV plot shows that the CdS devices are more strongly compensated within $\sim 0.4 \mu\text{m}$ of the junction, i.e. these devices have more shallow defects passivated in this region. Admittance spectroscopy indicates that nonpassivated defects have different activation energies, strongly suggesting that the Cd ions are not settling in the same lattice positions when they enter via CdS deposition as compared to entry via Cd PE treatment.

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