CIS Carrier-Density Profiles Derived from Capacitance

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ABSTRACT

This paper evaluates the use of capacitance-voltage (C-V) measurements on laboratory-scale polycrystalline thin-film CIS devices. In particular, the capacitance vs. frequency has been examined in a range spanning three decades, low temperature (- 50 ^oC) C-V measurements have been compared with room temperature (20 ^oC) measurements, and a variety of C-V pre-bias conditions have been compared. Also, C-V measurements made on devices with different buffer layers suggest that diffusion of cadmium from the window layer may cause greater compensation in the absorber.

1. Introduction

Earlier papers from our group discuss the measurement and interpretation of C-V measurements on polycrystalline thin-film CIS devices [1,2]. However, these were written when the typical efficiency for cells made from CIS was 8-10% [2]. Today, typical laboratory CIS cells are 14-16% efficient, and commonly include gallium and occasionally sulfur. Today's cells typically have carrier densities above 10^{16} cm^{-3}, compared to the 10^{15} cm^{-3} range for cells 10 years ago. In light of these higher efficiency cells with different dopant densities, the measurement technique and interpretation of C-V have been reevaluated.

Capacitance vs. frequency (C-F) measurements at four different bias voltages have been taken to confirm the validity of the use of the range of 1 kHz to 1000 kHz as standard practice. C-F and C-V have been measured at low temperatures, near room temperature, and various temperatures in between. C-V measurements have been taken after utilizing various pre-bias conditions to investigate the necessity for a 500 second reverse pre-bias. Finally, many measurements have been made on a variety of different CIS devices. We have chosen a small sample of these to present.

2. Measurement

The primary instrument used for measurements was a Hewlett-Packard 4192A LF Impedance Analyzer. Prior to all C-V measurements, C-F measurements were taken in the range of 1-1000 kHz within approximately 5 ^oC of the C-V measurement temperature. C-V measurements were taken with the voltage across the cell ranging from -2 V to 0.2 V. Unless otherwise noted, the cells were pre-biased for 500 seconds at a -2 V bias. All C-V measurements commenced at the pre-bias voltage. With the exception of the low temperature study, measurements were taken near 22 ^oC.

3. Results

C-F measurement results displayed in Figure 1 for the 1-400 kHz range are typical of most cells measured in that there is very little dispersion between 1 and 100 kHz. Below 0.5 kHz, a range not normally measured, there is significant scatter in the capacitance measurements. At frequencies near 200 kHz, the apparent capacitance increases, most likely due to the finite inductance of the measurement circuit [3]. Although moderate dispersion is occasionally present in C-F measurements, it can usually be attributed to shunting in the cell and is not a trait of well-behaved devices. Thus, for well-behaved devices we continue to see 1-1000 kHz as a reasonable range for standard C-F measurements.

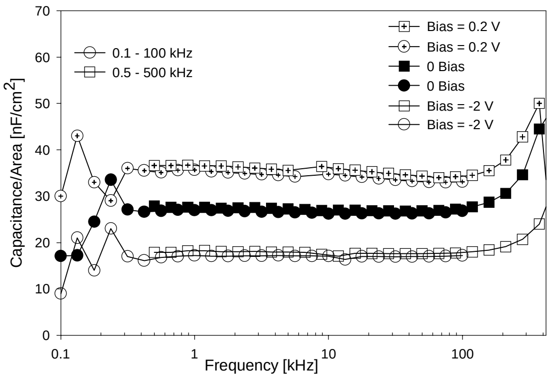

Fig. 1. C/A vs. F for a CIGSS/ CdS cell

Measurements taken incorporating variations of pre-bias duration and direction strongly suggest reverse-bias as the preferred pre-bias direction, but are not as conclusive regarding duration of the pre-bias. Reverse-bias was strongly indicated to be the preferred direction as a result of the curvature in the forward bias regime in the A^2/C^2 vs. V plots. For well-behaved diodes, the A^2/C^2 vs. V plots should have a voltage intercept approximately equal to the built-in voltage (V_{bi}), according to the following equation

$$A^2/C^2 = (2/q\varepsilon N)*(V_{bi}-V) \qquad (1)$$

Here q is the unit charge, ε is the dielectric constant of the absorber, and N is the carrier density of the more lightly doped material in the p-n junction [4]. However, as seen in Figure 2, plots extrapolated from C-V measurements made

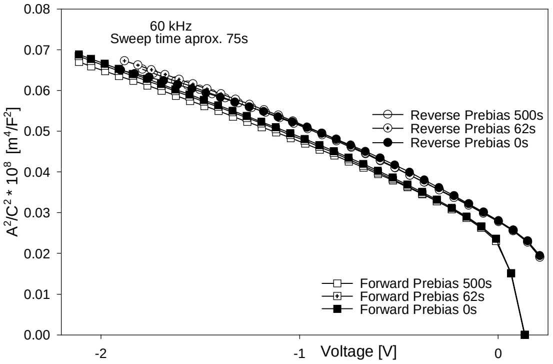

Fig. 2. C^2/A^2 vs. V from Reverse and Forward Prebias

after a forward pre-bias curved to zero at about 0.1 V, while the expected built-in voltage for CIS is between 0.5 and 1.0 V. Plots pertaining to measurements made after a reverse pre-bias on the same cell have a voltage intercept in the expected range of 0.5 to 1.0 V.

Investigations into C-V measurements made at low temperatures (- 50 °C) indicate several trends (Figure 3).

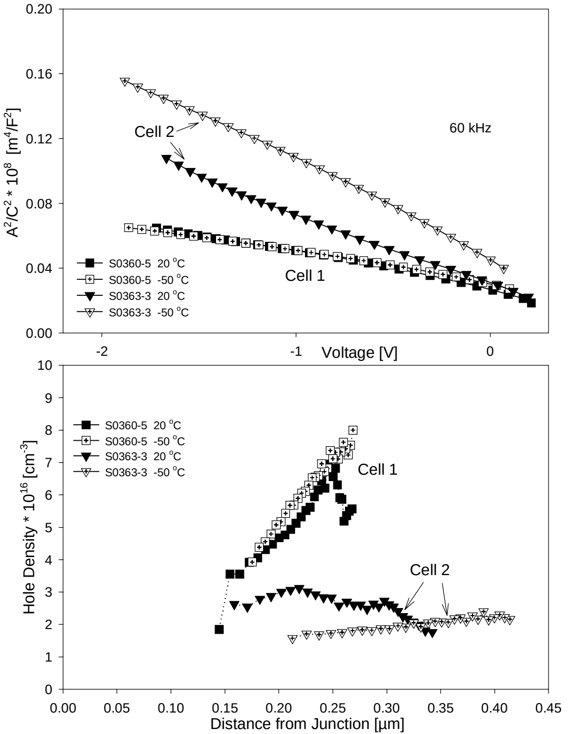

Fig. 3. A^2/C^2 vs. V and Carrier-Density Profiles for CIGSS Cells at Room and Low Temperature

Most significant is that between -50 °C and 20 °C, the overall carrier-density profile, which is calculated from the slope of the A^2/C^2 vs. V curve, did not change dramatically for any of the cells measured. Indeed, almost no dependence on temperature at all is seen for some cells. The low temperature and room temperature measurements in Figure 3 were taken on two CIS-based cells with NREL buffer layers made with slightly different processing steps. For these cells, more significant temperature variations exist when the capacitance at room temperature is lower. Note that even though the plots of A^2/C^2 vs. V seem to vary significantly with temperature in Figure 3 for cell 2, the carrier-density profiles are not dramatically different. This is consistent with low temperature measurements made on other CIS cells studied.

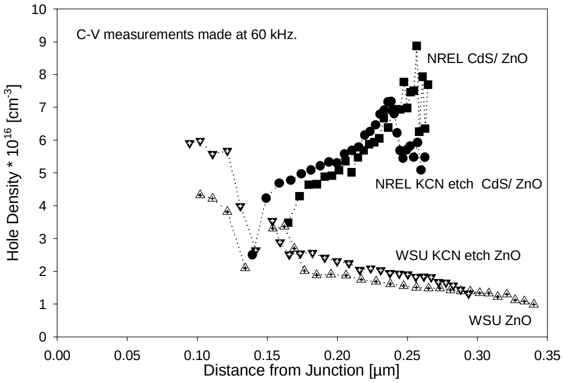

Fig. 4. Carrier-Density Profiles of CIGSS Thin-Film Devices

Finally, C-V measurements made on nominally identical CIGSS absorbers (Figure 4) suggest that compensation in completed devices with CdS buffer layers is less present in the cadmium-free completed devices. This is perhaps due to diffusion of the cadmium from the buffer layer or the buffer layer deposition process into this CIGSS absorber [5].

4. Acknowledgements

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